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What is claimed:

1. A pulse width control circuit for controlling a pulse width of an input signal based on pulse width control information, and generating an output signal for driving a light emitting element, comprising:

a rise/fall control section controlling at least one of a rise time and a fall time of said input signal according to a bit rate of said input signal;

a waveform shaping section shaping a signal output from said rise/fall control section, to generate said output signal; and

a control signal generating section generating a control signal controlling an operation of said rise/fall control section based on said pulse width control information;

wherein said rise/fall control section comprises:

a current source controlled in accordance with the control signal from said control signal generating section;

a bit detection element detecting a level of each bit indicated by said input signal;

an integrating element determining rise and fall time constants of said input signal based on a current supplied from said current source and detection results from said bit detection element;

wherein said current source includes:

a first current mirror circuit that is input with the control signal from said control signal generating section;

a second current mirror circuit that is input with an output signal of said first current mirror circuit;

a third current source having one terminal input with a power source voltage; and

an N-channel MOSFET having a gate terminal applied with the output signal of said first current mirror circuit, a drain terminal connected to the other terminal of said third current source, and a source terminal grounded;

said bit detection element includes:

a P-channel MOSFET having a gate terminal applied with said input signal, a source terminal applied with the power source voltage, and a drain terminal connected to an output terminal of said second current mirror circuit; and

an N-channel MOSFET having a gate terminal applied with said the input signal, a source terminal grounded, and a drain terminal connected to the other terminal of said third current source; and

said integrating element includes:

a first P-channel MOSFET having a drain terminal and a gate terminal each connected to the output terminal of said second current mirror circuit, and a source terminal applied with the power source voltage;

a first N-channel MOSFET having a drain terminal and a gate terminal each connected to the other terminal of the third current source, and a source terminal grounded;

a second P-channel MOSFET having a gate terminal connected to the output terminal of said second current mirror circuit, a source terminal applied with the power source voltage, and a drain terminal connected to an output terminal of said rise/fall control section; and

a second N-channel MOSFET having a gate terminal connected to the other terminal of the third current source, a source terminal grounded, and a drain terminal connected to the output terminal of said rise/fall control section.